ABSTRACT

To provide a data processor, which allows a CPU to access an external memory in an interval between data accesses from a DPS having a variable data length.

In a case where a 24-bit mode is set, when a determination section 11 determines that a DSP 2 is accessing an external memory 102, a control section 12 commands to place the access from a CPU to the external memory 102 in a wait state. In a case where a 16-bit mode is set, the control section 12 commands an address-data switching section 13, allowing the CPU 111 to access the external memory by utilizing a third bus cycle, which is free.